

Atty Docket No.: **JCLA8066**Serial No.: **10/065,380****REMARKS****Present Status of Patent Application**

Claims 1-6, 8 and 16-18 remain pending of which claims 1, 6, 16, 17 and 18 have been amended. It is believed that new matter adds by way of amendments made to claims 1, 6, 16, 17 and 18, or otherwise to the application. For at least the following reasons, Applicants respectfully submit that claims 1-6, 8 and 16-18 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of claim rejections

1. The Office Action rejected claims 1-6, 8 and 17-18 under 35 U.S.C. 102(e) as being anticipated by Kawahata et al. (US-6,356,318, hereinafter Kawahata).

In rejecting the above claims, the Office Action stated that Kawahata is silent about the upper (second) capacitor electrode having a surface area smaller than the lower (first) capacitor electrode. However, Figures 4, 5 and 6 clearly illustrate the upper (second capacitor electrode) having a surface area being smaller than the lower (first) capacitor electrode 7. Kawahata capacitor structure is identical as claims 1-6, 8 and 16-17. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to recognize that Kawahata's device could have solved problems caused by the residual conductive materials.

Applicants respectfully disagree with the Examiner's interpretation of Kawahata's capacitor structure shown in Figures 4, 5 and 6. Applicants have further amended Claims 1, 6,

Atty Docket No.: JCLA8066

Serial No.: 10/065,380

17 and 18 to specify that [the capacitor dielectric layer completely covers the first capacitor electrode and is in physical contact with the entire first capacitor electrode], wherein a (surface) area of the second capacitor electrode is smaller than a (surface) area of the first capacitor electrode, in order to clearly define the claimed invention.

To the contrary, Kawahata substantially teaches an active-matrix liquid crystal display comprising a gate insulating film 8 of a thickness in the range of 3000 to 5000 ANG. covering the gate lines 7 and 7' and the gate electrodes 7a. Next, openings 9 are formed in part of the gate insulating film 8 overlying the gate lines 7' in regions corresponding to storage capacitors Cs to form the storage capacitors Cs therein. An insulating film 10 for forming the storage capacitors Cs is formed on the gate insulating film 8. In other words, Kawahata, in FIG. 4, substantially shows an insulating film 10 is sandwiched between the lower electrode 7', and the upper electrode 15, wherein the gate insulating layer 8 partially covers the edges of the lower electrode 7'. Neither gate insulating film 8 nor insulating film 10 completely covers the lower capacitor electrode and in physical contact with the entire lower capacitor electrode 7'. Therefore it is evident that Kawahata fails to disclose a storage capacitor comprising at least "a capacitor dielectric layer completely covering the lower capacitor electrode and in physical contact with the entire lower capacitor electrode, wherein a (surface) area of the second (upper) capacitor electrode is smaller than a (surface) area of the first (lower) capacitor electrode, as required by claims 1, 16, 17 and 18". Accordingly, Applicants respectfully submit that Kawahata cannot anticipate claims 1, 6, 17 and 18 in this regard and therefore claims 1, 6, 17 and 18 should be allowed.

Atty Docket No.: JCLA8066

Serial No.: 10/065,380

For at least the forgoing reason, claims 1-6, 8 and 17-18 patentably distinguish over Kawahata. Reconsideration and withdrawal of these rejections is respectfully requested.

2. The Office Action rejected claim 16 under 35 U.S.C. 103(a) as being unpatentable over the Applicants' Admitted Prior Art (AAPA) in view of Kawahata.

Applicants respectfully disagree and would like to point out that AAPA besides failing to show a second capacitor electrode having an area smaller than an area of the first capacitor electrode, AAPA also fails to mention that the capacitor dielectric layer completely covers the first capacitor electrode and in physically contact with the entire first capacitor electrode, as required by the amended Claim 16. Further, as substantially discussed above, Kawahata substantially fails to disclose a storage capacitor comprising a capacitor dielectric layer that completely covers the first (lower) capacitor electrode and in physical contact with the entire first capacitor electrode, wherein an area of the second capacitor electrode is smaller than the area of the first capacitor electrode, as required by the amended Claim 16. Instead, Kawahata substantially teaches a storage capacitor comprising a capacitor dielectric layer (10) that is partially in physical contact with the lower capacitor electrode (7') while the edges thereof is covered by the insulating layer (8) as shown in FIG. 5. Accordingly, Applicants respectfully submit that no combination of AAPA and Kawahata can meet Claim 16 in this regard.

Further, Applicants respectfully submit that no amorphous Si residue will occur on the insulating film 10 during the patterning of the amorphous Si layer 12, which would otherwise cause the shorting of the upper electrode 15 and the neighboring signal line 14 if the surface area of the

Atty Docket No.: JCLA8066

Serial No.: 10/065,380

upper electrode 15 is larger than that of the lower capacitor electrode 7', as shown in FIG. 4 and 5 of Kawahata because the insulating film 10 is formed on the amorphous Si layer 14. In other words, even if any generated amorphous residue material during the patterning of the amorphous layer 14 occurs, the amorphous residue material will be covered by the subsequently formed insulating layer 10, and therefore, the problems of shorting between the upper capacitor electrode 15 and the neighboring signal lines cannot possibly occur regardless of the surface area of the upper capacitor electrode 15 with respect to the lower capacitor electrode 7'. In other words, Kawahata substantially fails to either explicitly or implicitly teach, suggest or disclose the problems due to amorphous residue materials generated during the patterning of the amorphous Si layer 14.

Further, there is no motivation to combine AAPA and Kawahata.

Accordingly, Applicants respectfully submit that Kawahata and AAPA either alone or in combination cannot possibly render the claimed invention obvious. Reconsideration and withdrawal of the above rejections is respectfully requested.

Atty Docket No.: JCLA8066

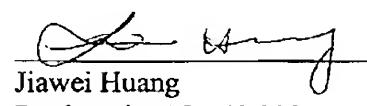
Serial No.: 10/065,380

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-6, 8 and 16-18 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
J.C. PATENTS

Date: 9/29/2003


Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949) 660-0809

RECEIVED
NEW YORK PAY CENTER

OFFICE

Page 10 of 10